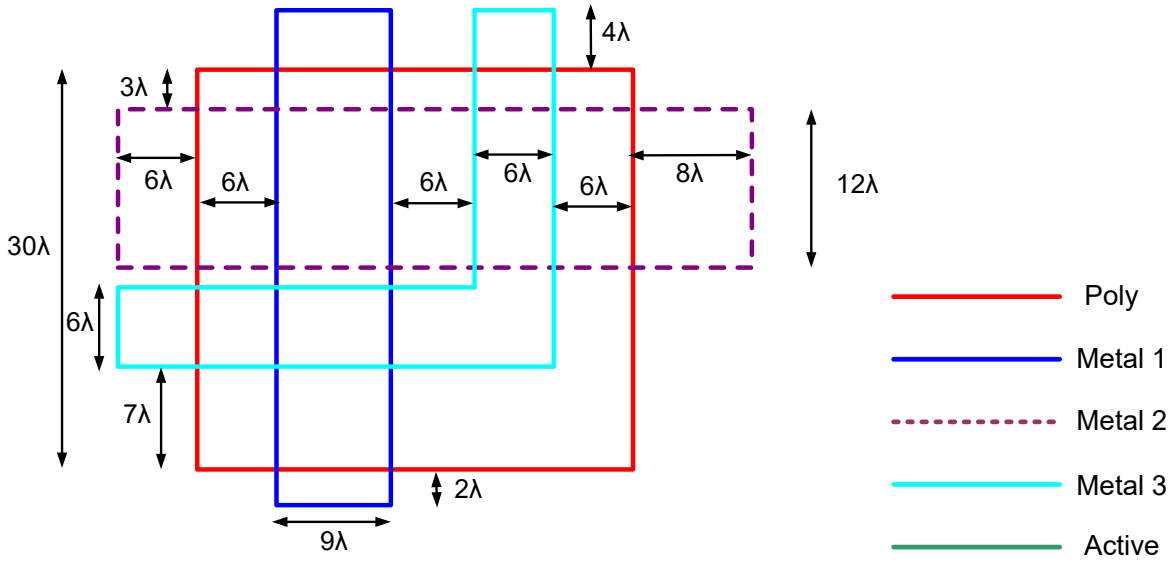
EE 330
Homework 5
Fall 2024 (This assignment is due Wednesday Sept 25 at noon. - late assignments not accepted this week)

Assume two CMOS processes are available, designated as either a 0.5µm or a 0.18µm process, that have the passive process parameters appended below. In each problem the specific process that is to be used will be specified. On those problems that involve the design of passive components, a sketch of the design is sufficient provided you indicate dimensions (i.e. it need not be done in Cadence).

Problem 1 Consider a Poly 1 interconnect in the 0.5 µm process that is 2λ wide and 400λ long. What is the resistance of this interconnect? What is the capacitance from this interconnect to the substrate? If Metal 1 is above this interconnect (and completely covers it in a top view), what is the capacitance between this interconnect and Metal 1? (recall λ=0.1μm for the 0.18µm process and λ=0.3μm for the 0.5µm process)

Problem 2 Assume a copper interconnect is 200µm long and 2µm wide and has a resistance of 20Ω. What is the sheet resistance and thickness? What length would a silver interconnect have to be for the same width, thickness and resistance?

Problem 3 Four non-contacting regions are shown. Identify the parasitic capacitances and their size if this is fabricated in the 0.5µm CMOS process. Don't forget that there is substrate below all layers.



Problem 4 Design a 3K resistor in the 0.5µm CMOS process. Use Poly 1 with a silicide block for the resistor (designated as HR-POLY). The width-length ratio of an

imaginary box enclosing the resistor should have a W/L ratio of between 1:3 and 3:1. The layout of the resistor can be either sketched or come from a Cadence layout.

Problem 5 Design a 150fF capacitor in the 0.5µm CMOS process. Clearly specify which layers you are using for this capacitor. The layout of the capacitor can be either sketched or come from a Cadence layout.

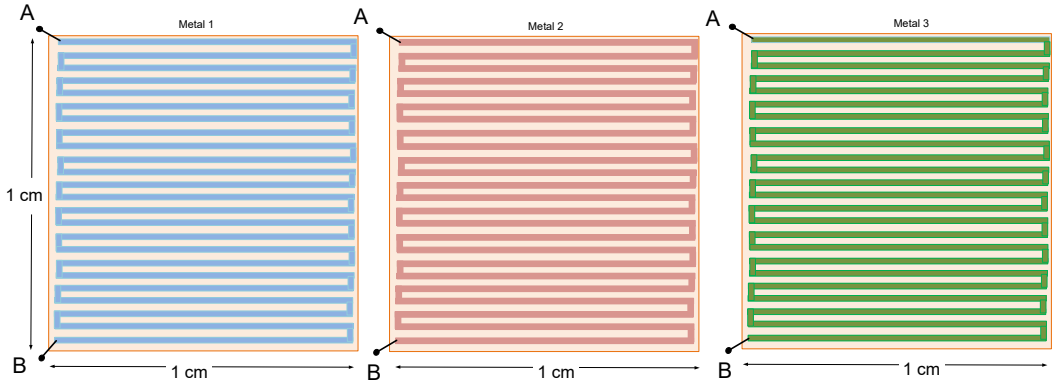
Problem 6 Consider an n+ diffused resistor that is 50u long and 4u wide. What is the nominal value of the resistance if it is doped with Arsenic and the doping density is 2E14/cm^3 (assume the diffusion depth is 0.1µm and the doping density is uniform throughout the region).

Problem 7 Consider a die that is 1cm on a side that has features on only the lowest 3 levels of metal designated as Metal 1, Metal 2, and Metal 3. These features form a resistor and are a simple serpentine pattern where the metal width is 0.1µm and the spacing is 0.1µm on each layer. This is depicted below (the width and spacing of the metal layers is not to scale). Assume the 3 resistors are connected in parallel and that the maximum permissible current that will not exceed the design rules is applied to this parallel combination. Assume the Design Rule Kit (DRC) specifies the maximum current density is 1.5mA/µm and the sheet resistance of all 3 metal layers is 0.12Ω/□.

a) Determine the total resistance between nodes A and B

b) Determine the maximum current that can be applied to this resistor

c) Determine the corresponding maximum power dissipation that will occur if the design rule limitations are not violated

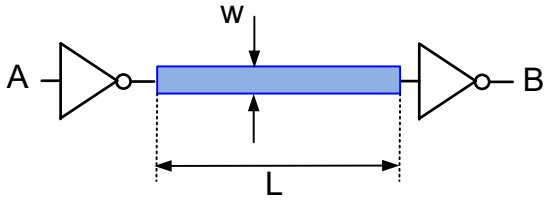


Problem 8 Consider two minimum-sized interconnected inverters designed in a 0.5µm CMOS process that are interconnected as shown below where the length of the interconnect is L and the width of the interconnect is W (W and L denote dimensions of the interconnect, not dimensions of the device in this problem). Assume the inverters are modeled with the switch-level model discussed in class that includes the effects of the thin-film inversion layer in the transistors when conducting.

a) Determine t_{HL} at the output of the first inverter if W=0.6µm and L=0.6µm and the interconnect is with M_1. Neglect the effects of any resistance in the interconnect.

b) Repeat part a) if L=200µm

c) Determine t_{HL} at the output of the first inverter if W=0.6µm and L=200µm and the interconnect is with Poly 1. Neglect the effects of any resistance in the interconnect.



Passive Process Parameters for 0.18µ CMOS Process								
	N+	P+	POLY	M1	M2	M3	N_W	UNITS
RESISTANCES								
Sheet Resistance	6.6	7.5	7.7	0.08	0.08	0.08	941	Ohms/sq
Contact Resistance	10.1	10.6	9.3		4.18	8.97		Ohms
CAPACITANCES								
Area (substrate)	998	1132	103	39	19	13	127	af/µm²
Area (N+ active)			8566[1]	54	21	14		af/µm²
Area (P+active)			8324[1]					af/µm²
Area (POLY)				64	18	10		af/µm²
Area (metal 1)					44	16		af/µm²
Area (metal 2)						38		af/µm²
Fringe (substrate)	244	201		18	61	55		af/µm
Fringe (poly)				69	39	29		af/µm
Fringe (metal 1)					64	35		af/µm
Fringe (metal 2)						54		af/µm
Overlap (P+active)			652					af/µm
[1] Transistor must be operating in triode or saturation for this parameter to be valid								

Passive Process Parameters for ON 0.5µm CMOS Process											
	N+	P+	POLY	POLY2	HR_POLY	M1	M2	M3	N/PLY	N_W	UNITS
RESISTANCES											
Sheet Resistance	84	105	23.5	999	44	0.09	0.10	0.05	825	815	Ohms/sq
Contact Resistance	65	150	17		29		0.97	0.79			Ohms
CAPACITANCES											
Area (substrate)	425	731	84			27	12	7		37	af/µm^2
Area (N+ active)			2434[1]			35	16	11			af/µm^2
Area (P+active)			2335[1]								af/µm^2
Area (POLY)				938		56	15	9			af/µm^2
Area (POLY2)						49					af/µm^2
Area (metal 1)							31	13			af/µm^2
Area (metal 2)								35			af/µm^2
Fringe (substrate)	344	238				49	33	23			af/µm
Fringe (poly)						59	38	28			af/µm
Fringe (metal 1)							51	34			af/µm
Fringe (metal 2)								52			af/µm
Overlap (N+active)			232								af/µm
Overlap (P+active)			312								af/µm
[1] Transistor must be operating in triode or saturation for this parameter to be valid											